Precision Instrumentation Amplifier

AD524

FEATURES
- Low Noise: 0.3 μV p-p 0.1 Hz to 10 Hz
- Low Nonlinearity: 0.003% (G = 1)
- High CMRR: 120 dB (G = 1000)
- Low Offset Voltage: 50 μV
- Low Offset Voltage Drift: 0.5 μV/°C
- Gain Bandwidth Product: 25 MHz
- Pin Programmable Gains of 1, 10, 100,1000
- Input Protection, Power On–Power Off
- No External Components Required
- Internally Compensated
- MIL-STD-883B and Chips Available
- 16-Pin Ceramic DIP and SOIC Packages and 20-Terminal Leadless Chip Carriers Available
- Available in Tape and Reel in Accordance with EIA-481A Standard
- Standard Military Drawing Also Available

PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

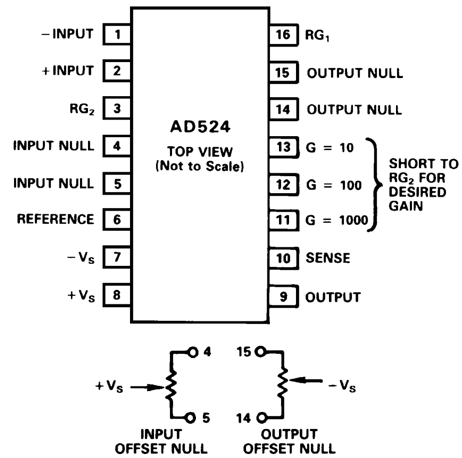
The AD524 has an output offset voltage drift of less than 25 μV/°C, input offset voltage drift of less than 0.5 μV/°C, CMR above 90 dB at unity gain (120 dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25 MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5 V/μs and settles in 15 μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

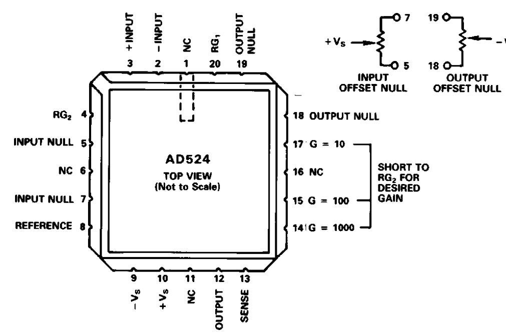
The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical “A” grade, the low drift “B” grade and lower drift, higher linearity “C” grade are specified from –25°C to +85°C. The “S” grade guarantees performance to specification over the extended temperature range –55°C to +125°C. Devices are available in 16-pin ceramic DIP and SOIC packages and a 20-terminal leadless chip carrier.

CONNECTION DIAGRAMS

Ceramic (D) and SOIC (R) Packages



Leadless Chip Carrier (E) Package



PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25 MHz, full power response of 75 kHz and a settling time of 15 μs to 0.01% of a 20 V step (G = 100).

REV. C

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Tel: 617/329-4700 Fax: 617/326-8703

AD524—SPECIFICATIONS (@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C unless otherwise noted)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$			$\left[\frac{40,000}{R_G}+1\right] \pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error[1]													
G = 1			**±0.05**			**±0.03**			**±0.02**			**±0.05**	%
G = 10			**±0.25**			**±0.15**			**±0.1**			**±0.25**	%
G = 100			**±0.5**			**±0.35**			**±0.25**			**±0.5**	%
G = 1000			**±2.0**			**±1.0**			**±0.5**			**±2.0**	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10,100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			**250**			**100**			**50**			**100**	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	mV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	**70**			**75**			**80**			**75**			dB
G = 10	**85**			**95**			**100**			**95**			dB
G = 100	**95**			**105**			**110**			**105**			dB
G = 1000	**100**			**110**			**115**			**110**			dB
INPUT CURRENT													
Input Bias Current			**±50**			**±25**			**±15**			**±50**	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			**±35**			**±15**			**±10**			**±35**	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_{DL})[2]	±10			±10			±10			±10			V
Max Common-Mode Linear (V_{CM})		$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$			$\mathbf{12\ V - \left(\frac{G}{2} \times V_D\right)}$		V
Common-Mode Rejection dc to 60 Hz with 1 kΩ Source Imbalance													
G = 1	**70**			**75**			**80**			**70**			dB
G = 10	**90**			**95**			**100**			**90**			dB
G = 100	**100**			**105**			**110**			**100**			dB
G = 1000	**110**			**115**			**120**			**110**			dB
OUTPUT RATING													
V_{OUT}, R_L = 2 kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal – 3 dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step													
G = 1 to 100		15			15			15			15		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1 kHz													
R.T.I.		7			7			7			7		nV/√Hz
R.T.O.		90			90			90			90		nV√Hz
R.T.I., 0.1 Hz to 10 Hz													
G = 1		15			15			15			15		µV p-p
G = 10		2			2			2			2		µV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		µV p-p
Current Noise													
0.1 Hz to 10 Hz		60			60			60			60		pA p-p

Model	Min	AD524A Typ	Max	Min	AD524B Typ	Max	Min	AD524C Typ	Max	Min	AD524S Typ	Max	Units
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ±20%
I_{IN}		15			15			15			15		µA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ±20%
I_{IN}		15			15			15			15		µA
Voltage Range	±10			±10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	–25		+85	–25		+85	–25		+85	–55		+125	°C
Storage	–65		+150	–65		+150	–65		+150	–65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA

NOTES
[1]Does not include effects of external resistor R_G.
[2]V_{OL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at the maximum = 10V/G.
V_D = Actual differential input voltage.
Example: G = 10, V_D = 0.50.
V_{CM} = 12 V – (10/2 × 0.50 V) = 9.5 V.

Specification subject to change without notice.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

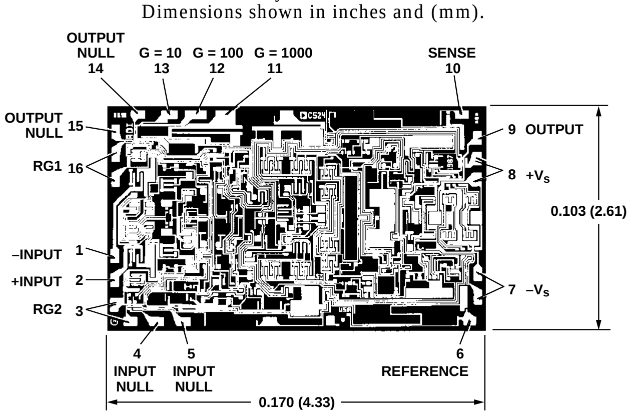
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation . . . . 450 mW
Input Voltage,[2]
(Either Input Simultaneously) $|V_{IN}| + |V_S|$ . . . . <36 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range
(R) . . . . –65°C to +125°C
(D, E) . . . . –65°C to +150°C
Operating Temperature Range
AD524A/B/C . . . .–25°C to +85°C
AD524S . . . . –55°C to +125°C
Lead Temperature (Soldering 60 secs) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Max input voltage specification refers to maximum voltage to which either input terminal may be raised with or without device power applied. For example, with ±18 volt supplies max V_{IN} is ±18 volts, with zero supply voltage max V_{IN} is ±36 volts.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



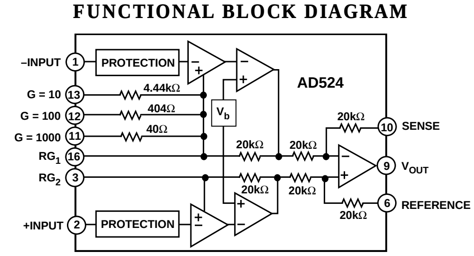
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D-16 AND R-16 16-PIN CERAMIC PACKAGES.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD524AD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524AE	–40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524AR-16	–40°C to +85°C	16-Pin Gull-Wing SOIC	R-16
AD524AR-16-REEL	–40°C to +85°C	Tape & Reel Packaging	
AD524BD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524BE	–40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524CD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524SD	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SD/883B	–55°C to +125°C	16-Pin Ceramic DIP	D-16
5962-8853901EA[1]	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SE/883B	–55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD524ACHIPS	–40°C to +85°C	Die	
AD524SCHIPS	–55°C to +125°C	Die	

[1]Refer to official DESC drawing for tested specifications.

FUNCTIONAL BLOCK DIAGRAM



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD524 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



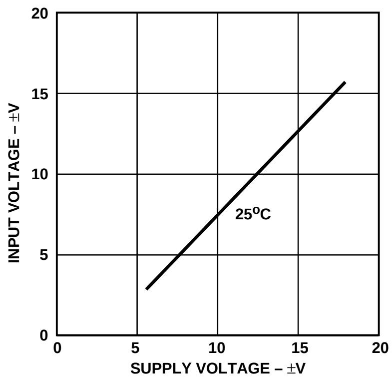


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

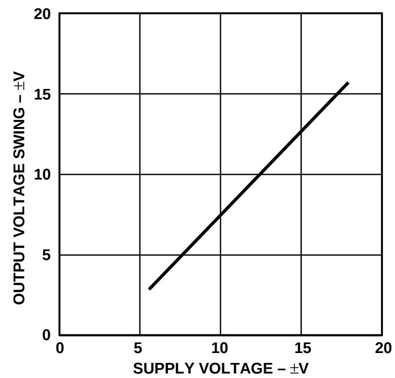


Figure 2. Output Voltage Swing vs. Supply Voltage

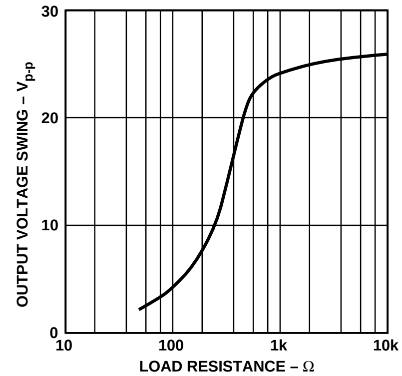


Figure 3. Output Voltage Swing vs. Load Resistance

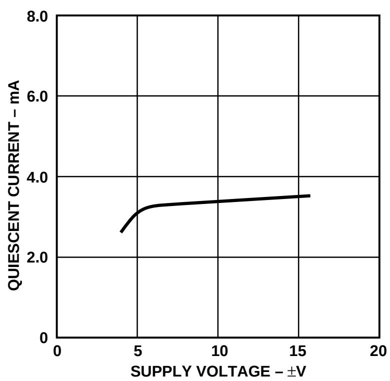


Figure 4. Quiescent Current vs. Supply Voltage

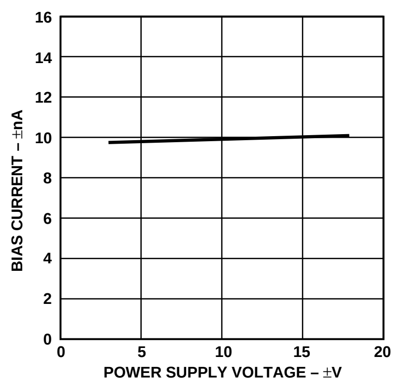


Figure 5. Input Bias Current vs. Supply Voltage

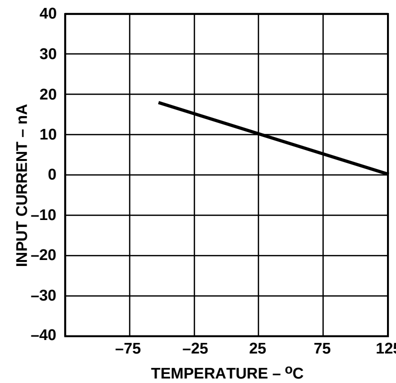


Figure 6. Input Bias Current vs. Temperature

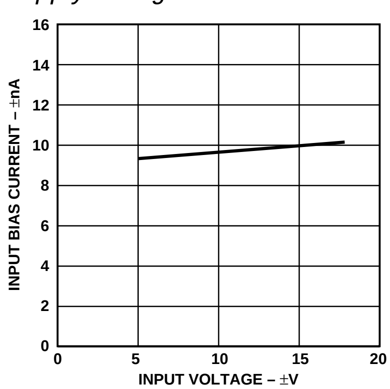


Figure 7. Input Bias Current vs. CMV

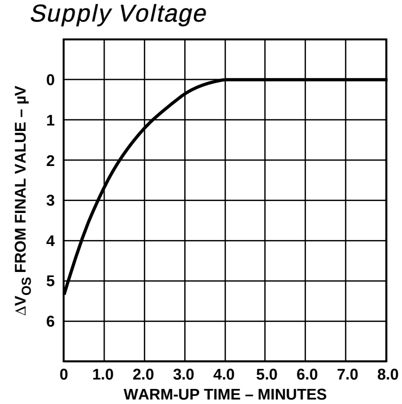


Figure 8. Offset Voltage, RTI, Turn On Drift

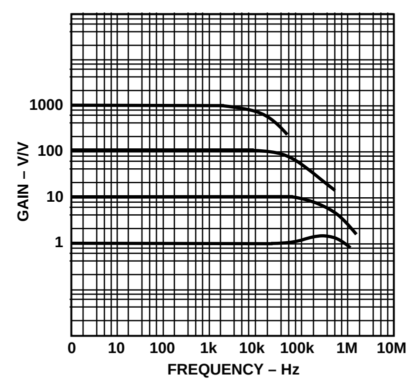


Figure 9. Gain vs. Frequency

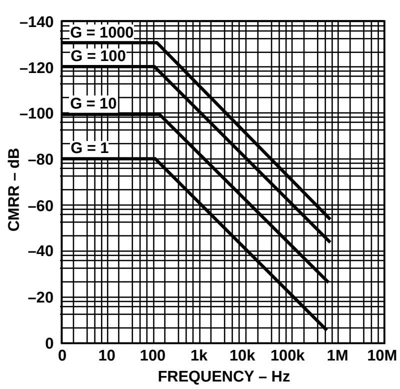


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

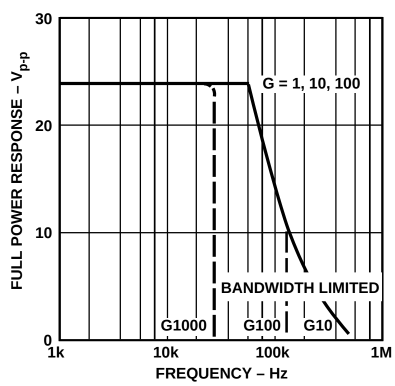


Figure 11. Large Signal Frequency Response

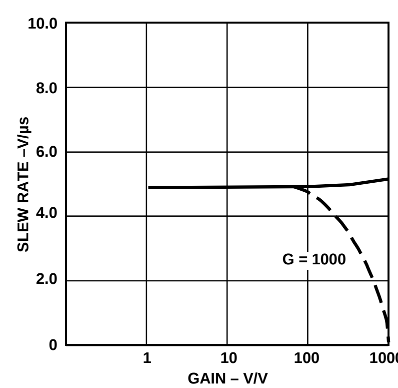


Figure 12. Slew Rate vs. Gain

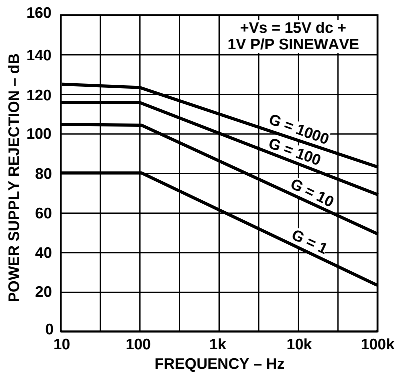


Figure 13. Positive PSRR vs. Frequency

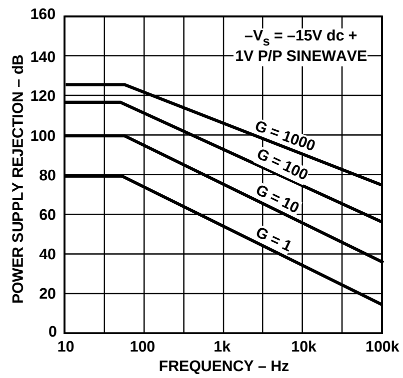


Figure 14. Negative PSRR vs. Frequency

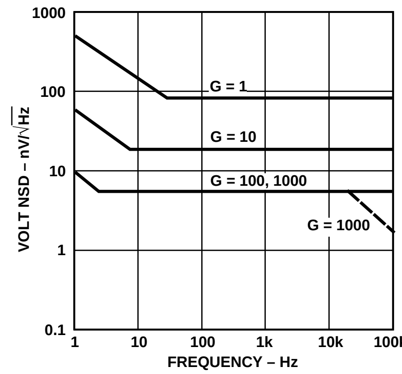


Figure 15. RTI Noise Spectral Density vs. Gain

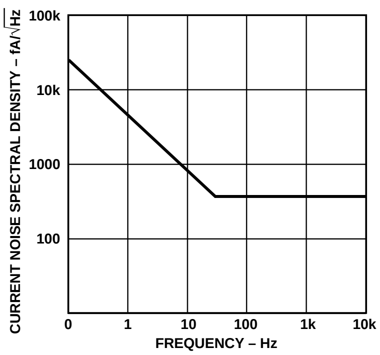


Figure 16. Input Current Noise

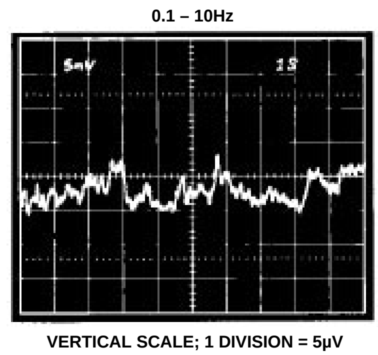


Figure 17. Low Frequency Noise – G = 1 (System Gain = 1000)

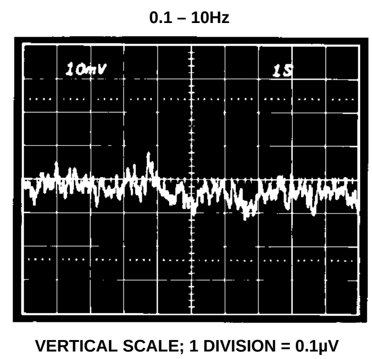


Figure 18. Low Frequency Noise – G = 1000 (System Gain = 100,000)

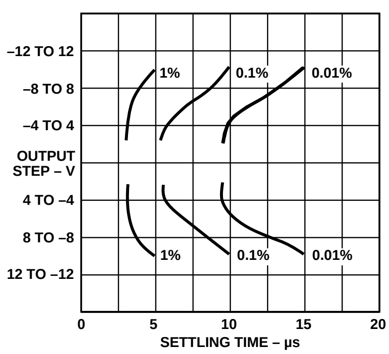


Figure 19. Settling Time Gain = 1

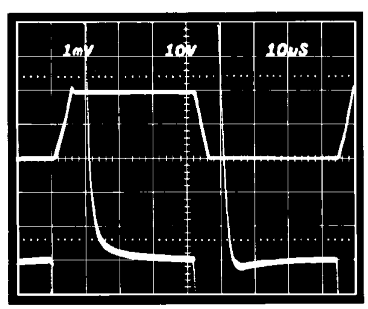


Figure 20. Large Signal Pulse Response and Settling Time – G =1

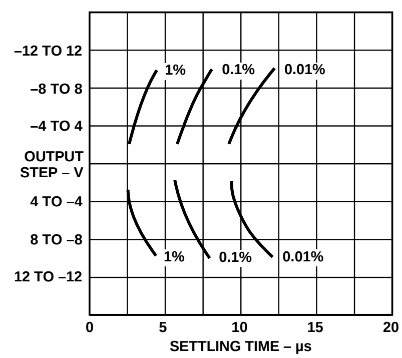


Figure 21. Settling Time Gain = 10

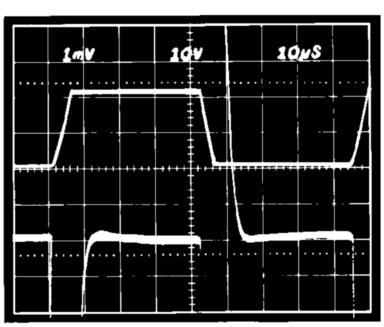


Figure 22. Large Signal Pulse Response and Settling Time G = 10

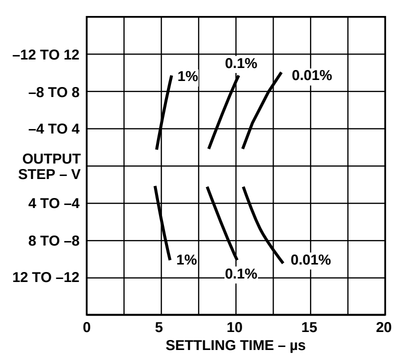


Figure 23. Settling Time Gain = 100

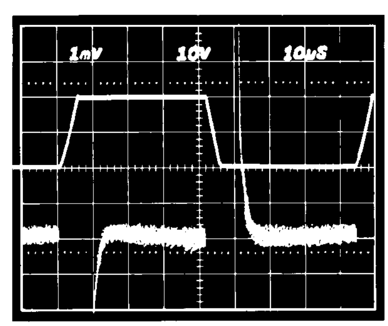


Figure 24. Large Signal Pulse Response and Settling Time G = 100

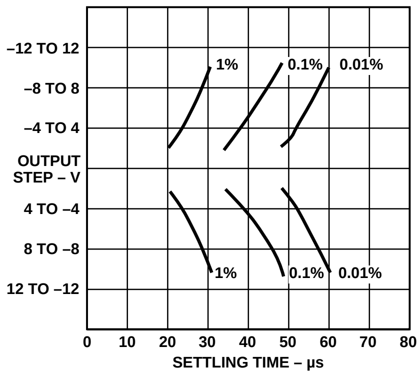


Figure 25. Settling Time Gain = 1000

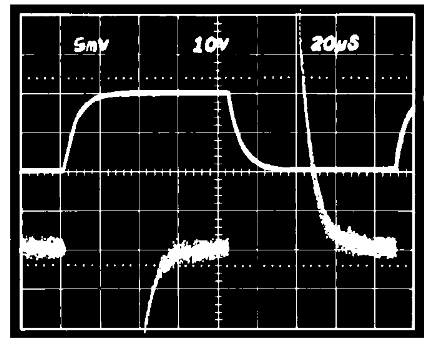


Figure 26. Large Signal Pulse Response and Settling Time G = 1000

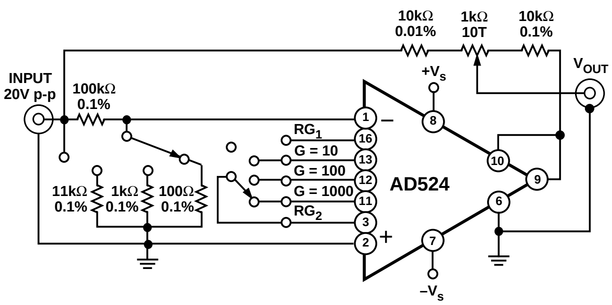


Figure 27. Settling Time Test Circuit

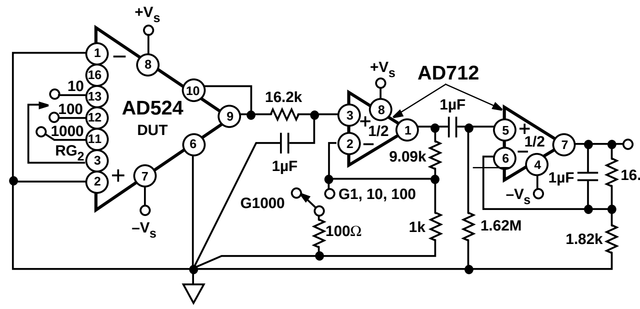


Figure 28. Noise Test Circuit

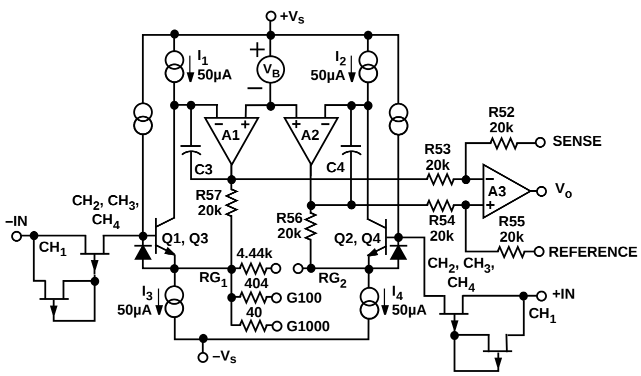


Figure 29. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 30ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25 MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of 7 nV/$\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5 mA with a full differential overload (36 V) would require over 7k of resistance which would add 10 nV$\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance (≈1 kΩ) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance (≈3 kΩ) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3 mA over the 36 V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250 μV output offset and a –50 μV input offset. In a unity gain configuration, the *total* output offset would be 200 μV or the sum of the two. At a gain of 100, the output offset would be –4.75 mV or: +250 μV + 100(–50 μV) = –4.75 mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G = 1 RG_2 is not connected).

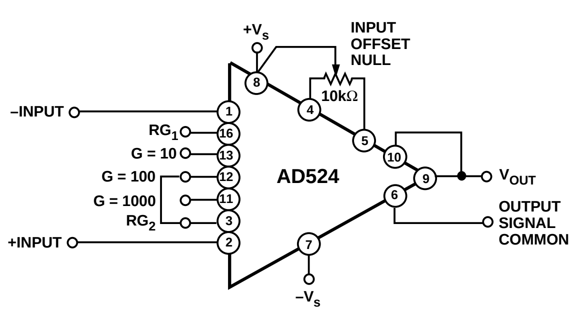


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16 which programs the gain according to the formula

$R_G = \frac{40k}{G = -1}$ (see Figure 31). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (– 50 ppm/°C typ).

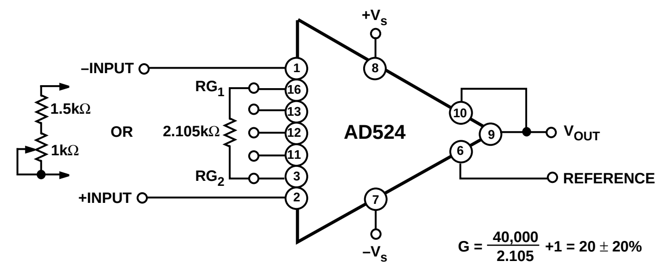


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

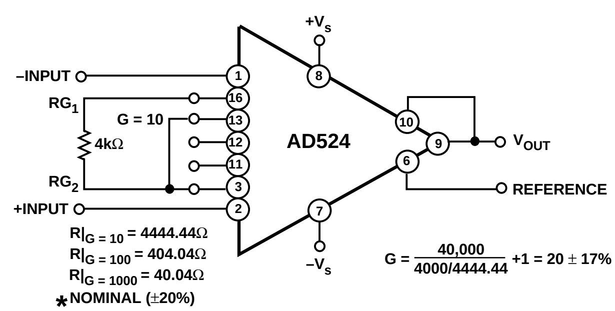


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

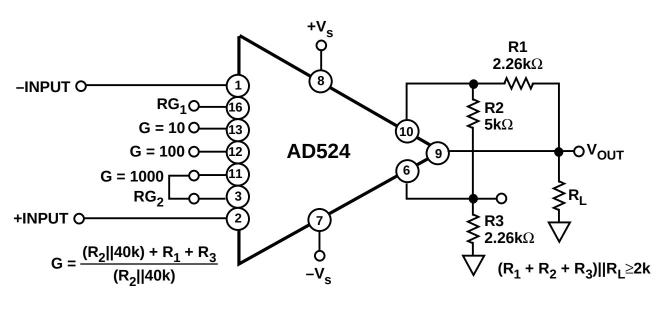


Figure 33. Gain of 2000

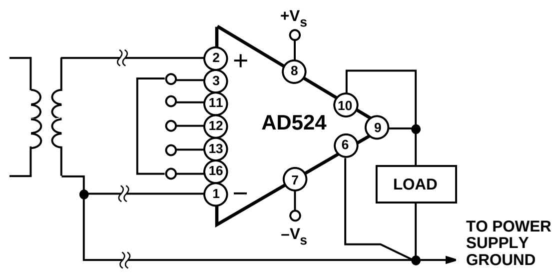
Table I. Output Gain Resistor Values

Output Gain	R2	R1, R3	Nominal Gain
2	5 kΩ	2.26 kΩ	2.02
5	1.05 kΩ	2.05 kΩ	5.01
10	1 kΩ	4.42 kΩ	10.1

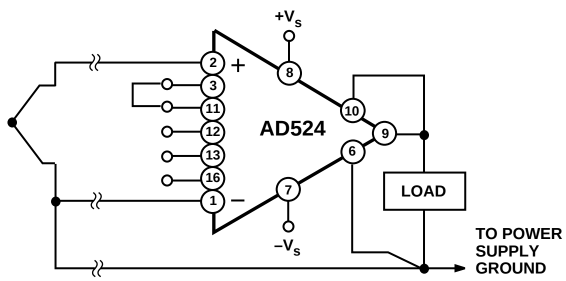
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

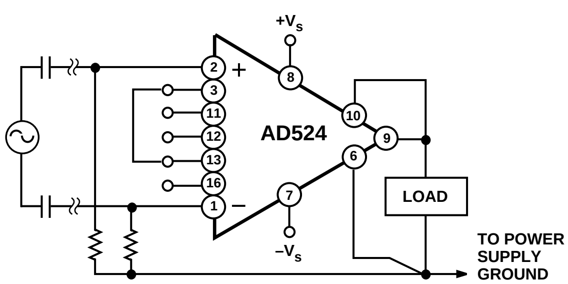
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying “floating” input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. “Common-Mode Rejection Ratio” (CMRR) is a ratio expression while “Common-Mode Rejection” (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards which are configured to improve ac common mode rejection by “bootstrapping” the capacitances of the input cabling, thus minimizing differential phase shift.

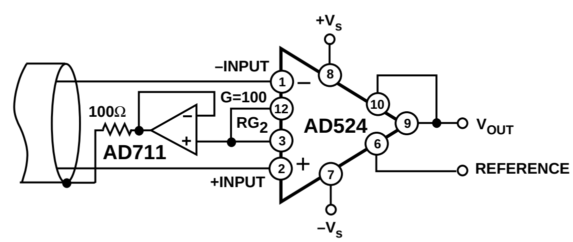


Figure 35. Shield Driver, G ≥ 100

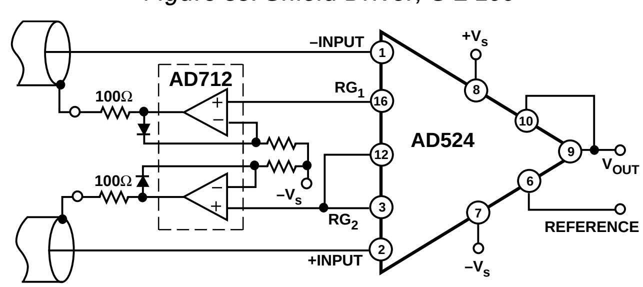


Figure 36. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground

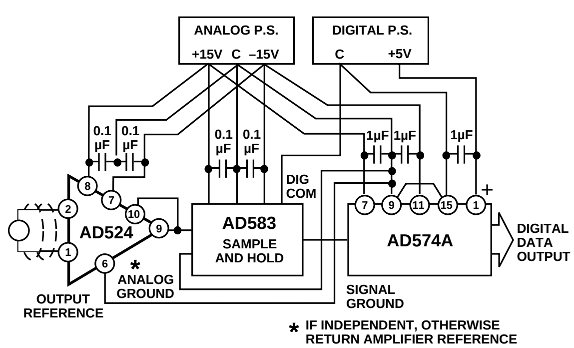


Figure 37. Basic Grounding Practice

wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

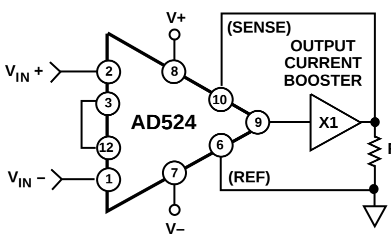


Figure 38. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2 kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 38 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10 V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset.

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal.

Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA.

In the AD524 a reference source resistance will unbalance the CMR trim by the ratio of 20 kΩ/R_{REF}. For example, if the reference source impedance is 1 Ω, CMR will be reduced to 86 dB (20 kΩ/1 Ω = 86 dB). An operational amplifier may be used to

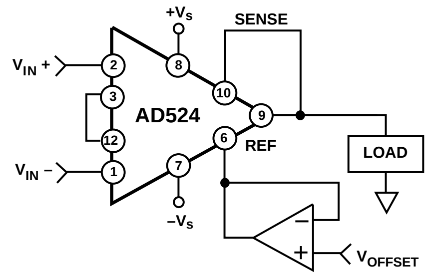
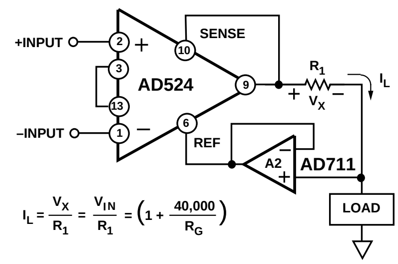


Figure 39. Use of Reference Terminal to Provide Output Offset

provide that low impedance reference point as shown in Figure 39. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 40.



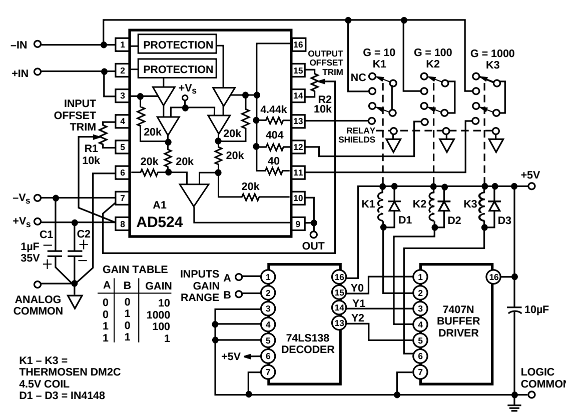
$$I_L = \frac{V_X}{R_1} = \frac{V_{IN}}{R_1} = \left(1 + \frac{40{,}000}{R_G}\right)$$

Figure 40. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 41 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.



A	B	GAIN
0	0	10
0	1	1000
1	0	100
1	1	1

Figure 41. Three Decade Gain Programmable Amplifier

The AD524 can also be connected for gain in the output stage. Figure 42 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common rejection ratio degradation.

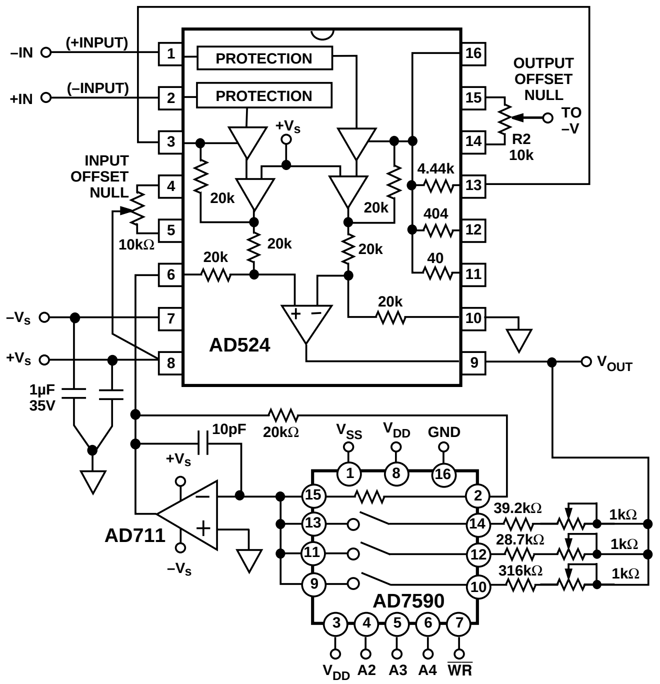


Figure 42. Programmable Output Gain

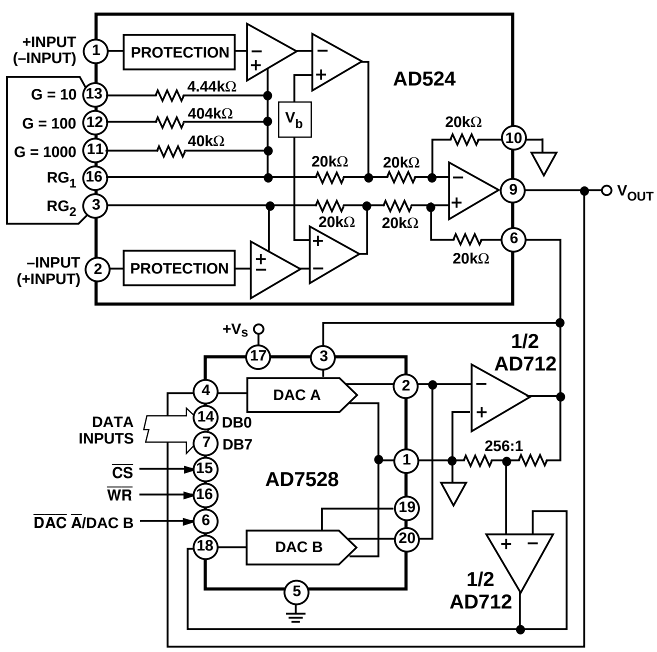


Figure 43. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 44 show a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

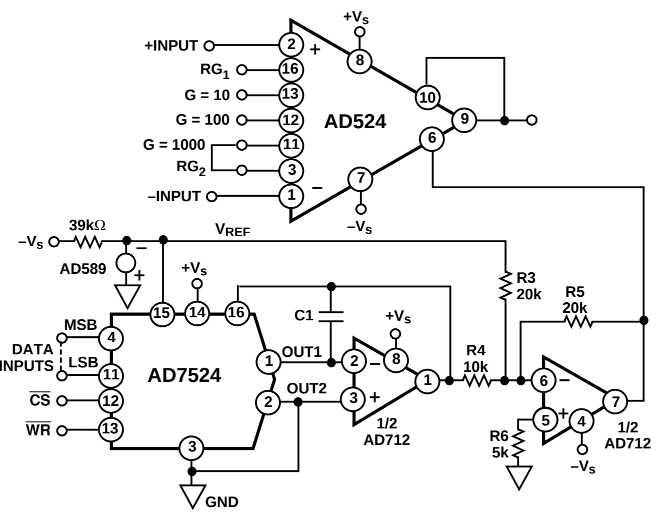


Figure 44. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For those applications Figure 45 provides a hardware solution.

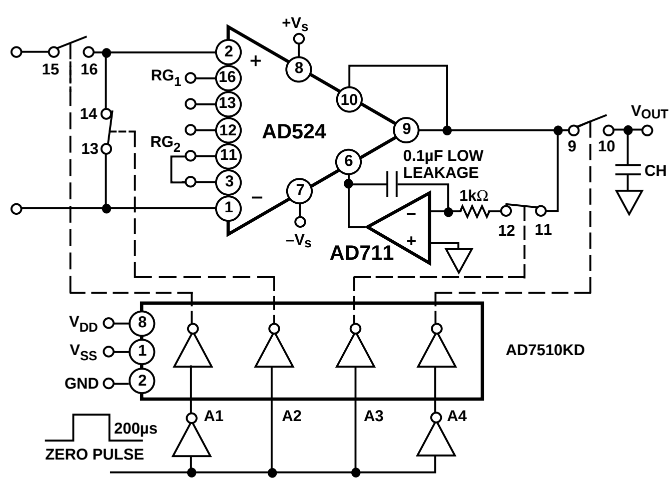


Figure 45. Auto-Zero Circuit

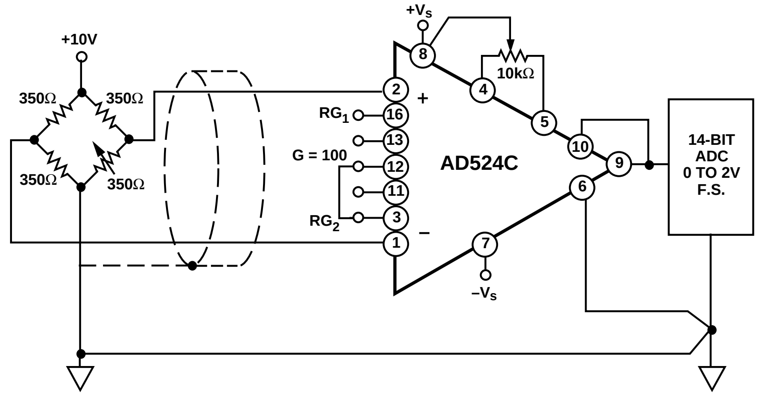


Figure 46. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100 Ω, supplying a 0 to 20 mV signal to an AD524C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is –25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C –25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

Table II. Error Budget Analysis of AD524CD in Bridge Application

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500 ppm	2500 ppm	2500 ppm	–
Gain Instability	25 ppm	(25 ppm/°C)(60°C) = 1500 ppm	–	1500 ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30 ppm	–	–	30 ppm
Input Offset Voltage	±50 µV, RTI	±50 µV/20 mV = ±2500 ppm	2500 ppm	2500 ppm	–
Input Offset Voltage Drift	±0.5 µV/°C –	(±0.5 µV/°C)(60°C) = 30 µV 30 µV/20 mV = 1500 ppm	–	1500 ppm	–
Output Offset Voltage[1]	±2.0 mV	±2.0 mV/20 mV = 1000 ppm	1000 ppm	1000 ppm	–
Output Offset Voltage Drift[1]	±25 µV/°C	(±25 µV/°C)(60°C)= 1500 µV 1500 µV/20 mV = 750 ppm	–	750 ppm	–
Bias Current-Source Imbalance Error	±15 nA	(±15 nA)(100 Ω) = 1.5 µV 1.5 µV/20 mV = 75 ppm	75 ppm	75 ppm	–
Bias Current-Source Imbalance Drift	±100 pA/°C	(±100 pA/°C)(100 Ω)(60°C) = 0.6 µV 0.6 µV/20 mV= 30 ppm	–	30 ppm	–
Offset Current-Source Imbalance Error	±10 nA	(±10 nA)(100 Ω) = 1 µV 1 µV/20 mV = 50 ppm	50 ppm	50 ppm	–
Offset Current-Source Imbalance Drift	±100 pA/°C	(100 pA/°C)(100 Ω)(60°C) = 0.6 µV 0.6 µV/20 mV = 30 ppm	–	30 ppm	–
Offset Current-Source Resistance-Error	±10 nA	(10 nA)(175 Ω) = 3.5 µV 3.5 µV/20 mV = 87.5 ppm	87.5 ppm	87.5 ppm	–
Offset Current-Source Resistance-Drift	±100 pA/°C	(100 pA/°C)(175 Ω)(60°C) = 1 µV 1 µV/20 mV = 50 ppm	–	50 ppm	–
Common Mode Rejection 5 V dc	115 dB	115 dB = 1.8 ppm × 5 V = 8.8 µV 8.8 µV/20 mV = 444 ppm	444 ppm	444 ppm	–
Noise, RTI (0.1 Hz–10 Hz)	0.3 µV p-p	0.3 µV p-p/20 mV = 15 ppm	–	–	15 ppm
		Total Error	6656.5 ppm	10516.5 ppm	45 ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple-iron(+)–constantan–is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

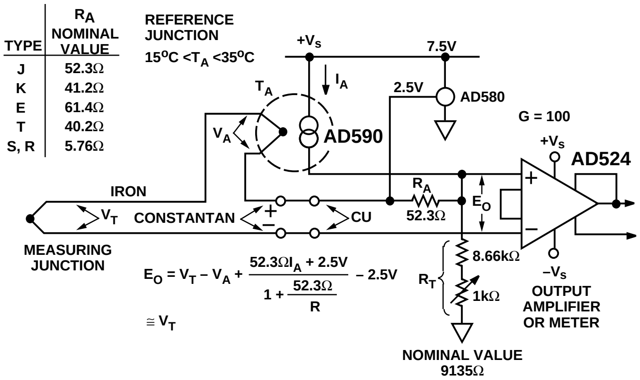


Figure 47. Cold-Junction Compensation

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

The microprocessor controlled data acquisition system shown in Figure 48 includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

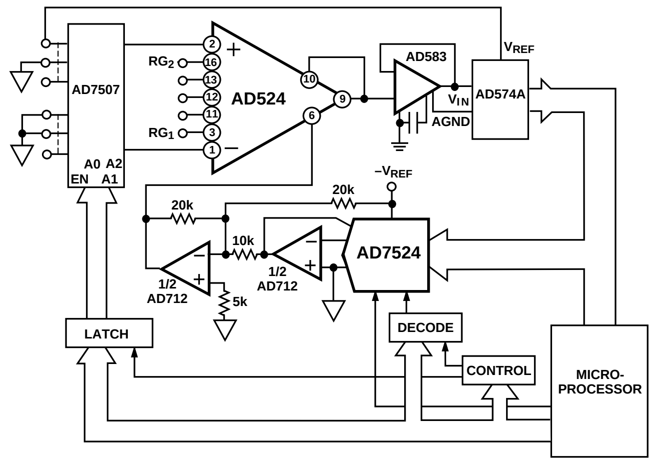


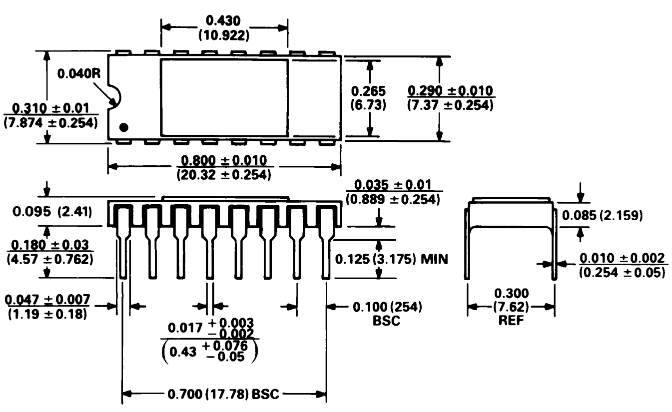
Figure 48. Microprocessor Controlled Data Acquisition System

For a comprehensive study of instrumentation amplifier design and applications, refer to the *Instrumentation Amplifier Application Guide*, available free from Analog Devices.

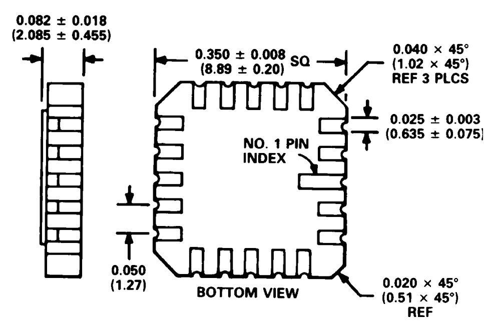
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Ceramic (D) Package



20-Terminal Leadless Chip Carrier (E) Package



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